1. A storage container structure comprising:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

2. A storage container structure comprising:

a substrate including a semiconductor structure;

a patterning stop region with a lower surface substantially coplanar with the top of said substrate;

an insulating overlayer over said substrate, said insulating overlayer comprising:

a lower overlayer surface positioned over said substrate, wherein said lower overlayer surface is in contact with said top of said substrate;

an upper overlayer surface, and

an intermediate overlayer portion defined between said lower overlayer surface and said upper overlayer surface;

a container region within said insulating overlayer, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom

wall, wherein all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

3. A storage container structure comprising:

a substrate including a semiconductor structure, said substrate including a generally planar upper surface;

an insulating overlayer disposed over and in contact with said generally planar upper surface of said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region including:

a lower surface substantially coplanar with said generally planar upper surface of said substrate; and

an upper surface configured such that the lowermost extension of said container bottom wall does not project substantially below said upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

4. A storage container structure comprising:

a substrate including a semiconductor structure, said substrate including a generally planar upper surface;

an insulating overlayer disposed over and in contact with said generally planar upper surface of said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region including:

a lower surface substantially coplanar with said generally planar upper surface of said substrate; and

an upper surface substantially coplanar with said container bottom wall;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.

5. A storage container structure according to claim 4, wherein said upper surface of said patterning stop region is configured such that all of said container bottom wall is defined by said upper surface of said patterning stop region.

6. A memory device comprising:

a storage container structure comprising:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region; and

a bit line terminal coupled to said charge storage lamina through a switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command.

7. A computer system comprising:

a storage container structure including:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a

container interior bounded in part by said container side walls and said container bottom wall;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region;

a bit line terminal coupled to said charge storage lamina through a switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command; and

a microprocessor in communication with a plurality of said charge storage structures via respective ones of a plurality of said bit line terminals.

8. A memory device comprising:

a storage container structure including:

a substrate including a semiconductor structure;

an insulating overlayer disposed over and in contact with said substrate, said insulating overlayer including a container region disposed therein, said container region defining a container cross section having container side walls, a container bottom wall, and a container interior bounded in part by said container side walls and said container bottom wall;

a transistor switching structure;

a patterning stop region disposed over said substrate such that all of said container bottom wall is defined by an upper surface of said patterning stop region, said patterning stop region forming part of said transistor switching structure;

a charge storage lamina over an interior surface of said container region;

a contact region defined by said charge storage lamina, wherein said contact region defines a contact region cross section having contact region side walls and a contact region bottom wall, and wherein said contact region side walls and said contact region bottom wall are defined by a first surface of said charge storage lamina; and

an electrical contact in said contact region, wherein respective portions of said electrical contact and said charge storage lamina occupy collectively at least a portion of said container region.; and

a bit line terminal coupled to said charge storage lamina through said switching structure, wherein a charge transfer status of said switching structure changes in response to a memory access command.